SECTION I—CLAIMS

Amendment to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application. Claims 1, 10-11, 14, 21-22, 24, and 30 are amended herein. Claims 4-5, 12-13, 15-17, 19-20, 23, and 25-27 are, or remain, canceled herein without prejudice. No new claims are added.

Listing of Claims:

1. (Currently amended) A processor readable~~, physical~~ medium having instructions stored thereon that, when executed by a processor in a switch, cause the switch to perform a method for implementing ~~encoding a data structure for supporting~~ one or more packet modification operations on a packet received at the switch, wherein the method comprises:~~, the data structure comprising:~~

~~a first pointer, entered in the data structure, to a sequence of commands, executable by a processor, implementing one or more packet modification operations and stored, in packed format, with more than one command stored in a single addressable entry of the stored sequence, in a first memory area; and~~

~~a second pointer, also entered in the data structure, to a burst of data or mask items, stored, in packed format, with more than one data or mask item stored in a single addressable entry of the stored burst, in a second memory area distinct from the first, for use by the processor in executing the one or more commands;~~

~~wherein the commands in the sequence specify performing the one or more packet modification~~

~~operations using, as operands or as masks for operands, the data or mask items in the burst.~~

associating a data structure link with the packet received at the switch by inserting a data structure index corresponding to the data structure link into a header of the packet;

retrieving a data structure from memory of the switch via the data structure link associated with the packet, wherein the data structure comprises:

a first pointer to a sequence of commands for execution by a processor of the switch to implement the one or more packet modification operations stored in packed format with more than one command stored in a single addressable entry in a sequence in a first memory area of the memory, and

a second pointer to a burst of data or mask items stored in packed format with more than one data or mask item stored in a single addressable entry in the stored burst in a second memory area of the memory distinct from the first memory area, the burst of data or mask items for use by the processor in executing the one or more commands;

retrieving the commands in the sequence from the first memory area via the first pointer;

retrieving the data or mask items in the burst from the second memory area via the second pointer; and

performing one or more packet modification operations on the packet by executing the commands in the sequence via the processor using the burst of data or mask items as operands or masks for operands in the one or more packet modification operations performed.

2. (Previously Presented) The processor readable medium of claim 1 wherein the first and second

memory areas are located in different memories.

3. (Previously Presented) The processor readable medium of claim 1 wherein the first and second memory areas are located in the same memory.

4-5. (Cancelled).

6. (Previously Presented) The processor readable medium of claim 1 wherein the data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Previously Presented) The processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip in relation to the processor.

8. (Previously Presented) The processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip in relation to the processor.

9. (Previously Presented) The processor readable medium of claim 1 wherein the data structure comprises a plurality of pointers, each to a sequence of commands implementing one or more packet modification operations.

10. (Currently amended) The processor readable medium of claim 9 wherein the data structure comprises a plurality of pointers, each to a burst of data or mask items.

11. (Currently amended) A method within a switch for ~~of~~ performing one or more packet modification operations on a packet received at the switch, wherein the method comprises: ~~associated with a data structure link, the method comprising:~~

associating a data structure link with the packet received at the switch by inserting a data structure index corresponding to the data structure link into a header of the packet;

retrieving a data structure from [[a]] memory of the switch via the data structure link associated with the packet, wherein ~~a data structure corresponding to the data structure link,~~ the data

structure ~~comprising~~ comprises:

a first pointer~~, entered in the data structure,~~ to a sequence of commands[[,]] for execution by a processor[[,]] of the switch to implement the ~~implementing~~ one or more packet modification operations~~, and~~ stored[[,]] in packed format[[,]] with more than one command stored in a single addressable entry in a ~~the stored~~ sequence [[,]] in a first memory area of the memory, and

a second pointer~~, also entered in the data structure,~~ to a burst of data or mask items[[,]] stored[[,]] in packed format[[,]] with more than one data or mask item stored in a single addressable entry in the stored burst[[,]] in a second memory area of the memory distinct from the first memory area, the burst of data or mask items for use by the processor in executing the one or more commands;

retrieving ~~from the first memory area~~ the commands in the sequence from the first memory area via ~~by using~~ the first pointer;

retrieving ~~from the second memory area~~ the data or mask items in the burst from the second memory area via ~~by using~~ the second pointer; and

~~executing the commands in the sequence by the processor, thereby~~ performing one or more packet modification operations on the packet by executing the commands in the sequence via the processor[[;]] using~~, as operands or as masks for operands in the one or more packet modification operations,~~ the burst of data or mask items ~~in the burst~~ as operands or masks for operands in the one or more packet modification operations performed.

12-13. (Canceled).

14. (Currently amended) The method of claim 11 wherein the first and second memory areas are: located in different and distinct physical memories;[[.]]

located in distinct portions of a same physical memory;

located in an internal recipe RAM (Random Access Memory) and an external SRAM (Static Random Access Memory) respectively;

located in a memory implemented off-chip from a modification processor to execute the sequence of commands; or

located in a memory implemented on-chip with the modification processor to execute the sequence of commands.

15-17. (Cancelled).

18. (Previously Presented) The method of claim 11 wherein the data or mask items in the burst comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19-20. (Cancelled).

21. (Currently amended) The method of claim ~~12~~ 11 wherein the data structure comprises a plurality of pointers, each to a sequence of commands implementing one or more packet modification operations.

22. (Currently amended) The method of claim ~~12~~ 11 wherein the data structure comprises a plurality of pointers, each to a burst of data or mask items.

23. (Cancelled).

24. (Currently amended) A packet modification system comprising:

an associator to associate a data structure link with a packet received at the packet modification system by inserting a data structure index corresponding to the data structure link into a header of the packet;

a memory to store ~~storing~~ a data structure comprising:

a first pointer~~, entered in the data structure,~~ to a sequence of commands implementing one or more packet modification operations and stored[[,]] in a first memory area of the memory in packed format[[,]] with more than one command stored in a single addressable entry in the stored sequence, ~~in a first memory area;~~ and

a second pointer~~, also entered in the data structure,~~ to a burst of data or mask items[[,]] stored[[,]] in a second memory area of the memory distinct from the first memory area in packed format[[,]] with more than one data or mask item stored in a single addressable entry in the stored burst; and ~~, in a second memory area distinct from the first, for use in the one or more packet modification operations; and~~

a processor ~~configured~~ to:

retrieve the commands in the sequence from the first memory area via the first pointer;

retrieve the data or mask items in the burst from the second memory area via the second pointer, and

execute the commands in the sequence ~~pointed to by the first pointer, using, as operands or masks of operands in the one or more packet modification operations, the data or mask items in the burst.~~ using the burst of data or mask items as operands or masks for operands in the one or more packet modification operations.

25-27. (Cancelled).

28. (Previously Presented) The system of claim 24 wherein the first and second memory areas are located in different memories.

29. (Previously Presented) The system of claim 24 wherein the first and second memory areas are located in the same memory.

30. (Currently amended) The system of claim 24 wherein the processor comprises a pipeline processor core ~~configured~~ to retrieve the commands in the sequence in a first stage, and execute the commands in the sequence in one or more subsequent stages.